(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 428 175 A1**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **90121916.2**

(51) Int. Cl.5: **G01P 15/12**, G01P 15/08

(22) Date of filing: **15.11.90**

(30) Priority: **15.11.89 JP 296728/89**

(43) Date of publication of application:
22.05.91 Bulletin 91/21

(84) Designated Contracting States:
DE FR GB

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(54) **Semiconductor sensor having funnel-shaped apertures in semiconductor substrate and method of making same.**

(57) A semiconductor sensor (20) with a compact structure is provided, which comprises a semiconductor substrate (21), a semiconductor diaphragm (23) integrally formed with the semiconductor substrate, and a penetrating aperture (27) formed in the semiconductor substrate so as to surround desired sides of the diaphragm. The aperture (27) has both a first funnel-shaped aperture (127) and a second funnel-shaped aperture (227) jointed to the first funnel-shaped aperture. A cavity (26) for defining the diaphragm (23) is provided when the semiconductor substrate (21) is subjected to electrolytic etching to form the second funnel-shaped aperture (227) therein.

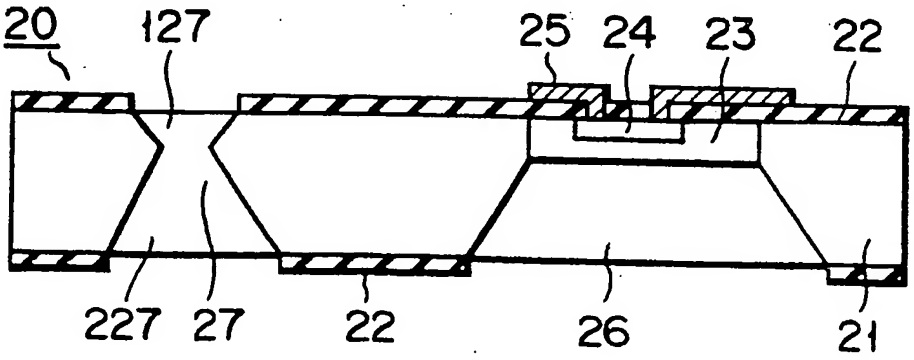

FIG. 4

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SEMICONDUCTOR SENSOR HAVING FUNNEL-SHAPED APERATURES IN SEMICONDUCTOR SUBSTRATE AND METHOD OF MAKING SAME

The present invention relates to a semiconductor sensor such as semiconductor acceleration sensors, semiconductor flow sensors and semiconductor micro-valves, and a method of making the same.

In semiconductor sensors such as semiconductor acceleration sensors, semiconductor flow sensors and semiconductor micro-valves, a silicon semiconductor ubstrate is selectively etched to provide a thin portion or a penetrating aperture therein. As a technique of etching such a silicon semiconductor substrate, there has been employed an electrolytic etching method using caustic potash, which utilizes a difference in electrolytic potentials due to the conductivity types of the semiconductor substrate. Fig. 1 shows etching characteristics obtained when N-type and P-type silicon semiconductor substrates having a (100) plane are electrolytically etched using the caustic potash. In Fig. 1, the ordinate indicates the electric current, and the abscissa the voltage, respectively. As is apparent from Fig. 1, in the case of the N-type semiconductor, the etching proceeds until the voltage reaches about 2 V. When the voltage exceeds 2 V, the etching is stopped. On the other hand, in the case of the P-type semiconductor, the etching proceeds until the voltage rises to about 4 V, but the etching stops when the voltage exceeds 4V. Thus, if the voltage is set at 3 V, the N-type semiconductor is not etched, while the P-type semiconductor is etched.

By means of this anisotropic etching, the thin portion or penetrating aperture is formed in the silicon semiconductor substrate, thus providing a semiconductor sensor. Fig. 2 shows a structure of a conventional semiconductor acceleration sensor, which comprises a P-type silicon semiconductor substrate 11, an N-type semiconductor region 13 serving as a thin portion (diaphragm) and formed in a major surface of the P-type semiconductor substrate 11, a P-type semiconductor region 14 serving as a resistor and formed in the N-type semiconductor region 13, an electrode wiring layer 15 formed on the P-type semiconductor region 14 through an insulating layer 12, a funnel-shaped cavity 16 made from the bottom surface of the semiconductor substrate 11 to form the thin portion, and a funnel-shaped aperture 17 penetrating in the thickness direction of the substrate 11 so as to surround both side surfaces of the thin portion.

The funnel-shaped aperture 17 is formed by etching the bottom surface of the semiconductor substrate 11 so as to penetrate the substrate 11. The angle between the bottom surface of the semiconductor substrate 11 and the wall defining the aperture 17 is about 60°. Thus, as is shown in Fig. 3, when the thickness of the semiconductor substrate 11 is given by h, the diameter of the funnel-shaped aperture 17 becomes 1.2 h. As a result, it is not possible to reduce the size of the semiconductor sensor.

It is, therefore, an object of the present invention to provide a semiconductor sensor for eliminating the disadvantage of the prior art.

Another object of the prsent invention is to provide a method of making a semiconductor sensor, wherein a funnel-shaped penetrating aperture and a diaphragm are simultaneously formed.

According to an aspect of the present invention, there is provided a semiconductor sensor with a compact structure, which comprises a semiconductor substrate, a semiconductor diaphragm integrally formed with the semiconductor substrate, and a penetrating aperture formed in the semiconductor substrate so as to surround desired sides of the diaphragm. The aperture has a first funnel-shaped aperture and a second funnel-shaped aperture jointed to the first funnel-shaped aperture. A cavity for defining the diaphragm is provided when the semiconductor substrate is subjected to electrolytic etching to form the second funnel-shaped aperture therein.

According to another aspect of the present invention, there is provided a method of making the semiconductor sensor according to a principle incorporated in the firstly referred aspect of the present invention.

The novel and distinctive features of the invention are set forth in the claims appended to the present application. The invention itself, however, together with further objects and advantages thereof may best be understood by reference to the following description and accompanying drawings in which:

Fig. 1 is a graph showing etching characteristics obtained when a silicon semiconductor substrate is electrolytically etched, using an electrolytic etching solution of caustic potash;

Fig. 2 is a cross-sectional view showing a conventional semiconductor acceleration sensor;

Fig. 3 is an enlarged cross-sectional view showing a funnel-shaped penetrating aperture in the conventional semiconductor acceleration sensor;

Fig. 4 is an enlarged cross-sectional view showing a semiconductor acceleration sensor according to an embodiment of the present invention;

Fig. 5 is a plane view of the semiconductor acceleration sensor;

Figs. 6A to 6D are cross-sectional views illustrating a process of making the semiconductor acceleration sensor according to the embodiment of the invention;

Fig. 7 is an enlarged cross-sectional view showing a funnel-shaped penetrating aperture in the semiconductor acceleration sensor according to the embodiment of the invention; and

Figs. 8A to 8C are enlarged cross-sectional views showing various types of funnel-shaped penetrating apertures in the semiconductor sensors.

A semiconductor acceleration sensor according to an embodiment of the present invention will now be described with reference to Figs. 4 and 5.

A semiconductor acceleration sensor 20 includes a P-type silicon semiconductor substrate 21, an N-type semiconductor region 23 serving as a thin portion (diaphragm) formed in a major surface of the P-type semiconductor substrate 21, P-type semiconductor regions 24 formed in the N-type semiconductor region 23 and serving as resistor layers, electrode wiring layers 25 formed above the P-type semiconductor regions 24 through an insulating layer 22, and a funnel-shaped cavity 26 formed from the bottom surface of the semiconductor substrate 21 and defining the thin portion. A funnel-shaped aperture 27 penetrating the substrate 21 in the thickness direction so as to surround the thin portion includes an upper aperture 127 formed from the top surface of the semiconductor substrate 21 and a lower aperture 227 formed from the bottom surface of the substrate 21. As is shown in Fig. 5, in the semiconductor acceleration sensor 20, four P-type semiconductor regions 24 serving as resistor layers are provided in the N-type semiconductor region 23 serving as the diaphragm in order to provide a bridge circuit. Though not shown, bonding pads are formed at an end portion of the semiconductor substrate 21. The bonding pads are connected to end portions of the resistor layers 24 through the electrode wiring layers 25.

A method of making the semiconductor acceleration layer 20 will now be described with reference to Figs. 6A to 6D.

As is shown in Fig. 6A, a P-type silicon semiconductor substrate 21 having a thickness of 300 microns and having a (100) or (110) crystal plane is prepared. Oxide films 122 and 222 are formed on both surfaces of the semiconductor substrate 21. An N-type impurity is selectively introduced into the semiconductor substrate to provide an N-type semiconductor region 23 having a thickness of 60 to 80 microns therein. Then, a P-type impurity is introduced into the N-type semiconductor region 23, thereby forming a plurality of P-type semiconductor regions 24 serving as resistors. For example, each of the P-type semiconductor regions 24 has a depth of about 3 microns, a length of about 80 microns, and a width of about 20 microns.

As is shown in Fig. 6B, after an opening with a predetermined size is formed in the oxide film 122, electrolytic etching with use of an electrolyte of caustic potash is carried out to form an upper funnel-shaped aperture 127 in the substrate 21. In this case, the depth of the funnel-shaped aperture 127 is set so as to be equal to the thickness of the N-type semiconductor region 23.

Subsequently, as is shown in Fig. 6C, the oxide film 122 on the P-type semiconductor region 24 is selectively removed to provide electrode wiring layers 25 at both end portions of the P-type semiconductor region 24.

Then, as is shown in Fig. 6D, openings of predetermined sizes are made in the oxide film 222 formed on the bottom surface of the semiconductor substrate 21 at positions corresponding to the funnel-shaped aperture 127 and the N-type semiconductor region 23. In the same manner as mentioned above, the exposed semiconductor substrate 21 is selectively removed by the electrolytic etching, thereby forming a lower funnel-shaped aperture 227 and a cavity 26 therein. In this case, the funnel-shaped apertures 127 and 227 are connected with each other, and a penetrating aperture 27 is formed. In addition, a diaphragm or a thin portion (corresponding to the N-type semiconductor region 23) is formed by the cavity 26. As a matter of course, in the described etching steps, the semiconductor substrate 21 is coated with an etching mask such as wax materials.

As is clear from Fig. 6D, the angle between the bottom surface of the semiconductor substrate 21 (having a length of about 6 mm) and the wall defining the aperture 227 is about 60°. The diameter of the opening of the aperture 127 is about 0.35 mm, that of the opening of the aperture 227 is about 0.5 mm, and that of the opening of the cavity 26 is about 1 mm, respectively.

Fig. 7 is an enlarged cross-sectional view showing the penetrating aperture 27 consisting of the funnel-shaped apertures 127 and 227 shown in Fig. 6D. When the depth of the aperture 127 is given by h/4 (h: the thickness of semiconductor substrate 21), the diameter of the opening of the funnel-shaped aperture 227 becomes 0.9 h. Thus, the size of the penetrating aperture 27 can be reduced, as compared with the prior art shown in Fig. 3 wherein only the bottom surface of the substrate is etched to form the funnel-shaped aperture.

The funnel-shaped apertures 127 and 227 formed at both side portions of the diaphragm serve as buffers against mechanical and thermal shock.

Furthermore, as is shown in Figs. 8A to 8C; penetrating apertures provided by upper and lower funnel-shaped apertures 127 and 227 having various configurations, which are different in the diameter and depth may be formed in the semiconductor substrate, and diaphragms having the different thickness, that is, the different depth may also be provided.

As has been described above, according to the present invention, since the penetrating aperture in the semiconductor substrate is provided by upper and lower funnel-shaped apertures which are formed from both surfaces of the substrate by means of etching, the size of the penetrating aperture can be reduced, and the lower funnel-shaped aperture and the cavity can be simultaneously formed with high precision. In addition, by changing the etching amount of the top and bottom surfaces of the substrate, the thickness of the diaphragm can be controlled. Therefore, high sensitivity semiconductor sensors with the small size can be obtained with a high yield.

It is further understood by those skilled in the art that the foregoing description is a preferred embodiment of the disclosed device and the method and that various changes and modifications may be made in the invention departing from the spirit and scope thereof.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor sensor (20) comprising a semiconductor substrate (21) of one conductivity type having upper and lower surfaces, and a semiconductor diaphragm (23) integrally formed with said semiconductor substrate,
characterized in that a penetrating aperture (27) having a funnel-shaped structure in said upper and lower surfaces is provided in said semiconductor substrate so as to surround desired sides of said diaphragm.

2. The semiconductor sensor according to claim 1, characterized in that said semiconductor substrate (21) is of P-type conductivity.

3. The semiconductor sensor according to claim 1, characterized in that said diaphragm (23) has one conductivity type opposite to said semiconductor substrate.

4. The semiconductor sensor according to claim 1, characterized in that said diaphragm (23) has a same conductivity type as said semiconductor substrate.

5. The semiconductor sensor according to claim 1, characterized in that said penetrating aperture includes a first funnel-shaped aperture (127) formed from said upper surface of said semiconductor substrate, and a second funnel-shaped aperture (227) formed from said lower surface thereof.

6. The semiconductor sensor according to claim 5, characterized in that said penetrating aperture (27) surrounds desired sides of said diaphragm (23).

7. The semiconductor sensor according to claim 5, characterized in that a depth of said first funnel-shaped aperture (127) is shallower than that of said second funnel-shaped aperture (227).

8. The semiconductor sensor according to claim 1, characterized in that said diaphragm (23) includes diffused resistors (24).

9. A method of making a semiconductor sensor (20) having a diaphragm (23) formed in a semiconductor substrate (21) of one conductivity type, characterized in that said semiconductor substrate (21) is selectively etched to a desired depth from an upper surface thereof to provide a first funnel-shaped aperture (127) therein; and that said semiconductor substrate (21) is selectively etched from a lower surface thereof until reaching said first funnel-shaped aperture (127), thereby providing both a second funnel-shaped aperture (227) jointed to said first funnel-shaped aperture (127) and a cavity (26) for defining said diaphragm (23) therein at the same time.

10. The method according to claim 9, characterized in that said first and second funnel-shaped apertures (127, 227) provide a penetrating aperture (27).

11. The method according to claim 10, characterized in that said penetrating aperture (27) surrounds desired sides of said diaphragm (23).

12. The method according to claim 9, characterized in that an impurity having one conductivity type opposite to that of said diaphragm (23) is selectively introducing into said diaphragm to provide diffused resistors (24) therein.

13. A method of making a semiconductor sensor (20) having a diaphragm (23) in a semiconductor substrate, characterized by:
preparing a P-type semiconductor substrate (21) having upper and lower surfaces;
selectively introducing an N-type impurity into said semiconductor substrate from said upper surface to provide an N-type semiconductor region (23) for a diaphragm;
forming P-type semiconductor elements (24) in said N-type semiconductor region;
subjecting said semiconductor substrate (21) to electrolytic etching from said upper surface to form a first funnel-shaped aperture (127) surrounding desired sides of said N-type semiconductor region (23); and
subjecting said semiconductor substrate (21) to electrolytic etching from said lower surface to form both a second funnel-shaped aperture (227) jointed

to said first funnel-shaped aperture (127) and a cavity (26) for defining said diaphragm.

14. The method according to claim 13, characterized in that said semiconductor substrate (21) has a (100) plane.

15. The method according to claim 13, characterized in that said electrolytic etching is carried out by using caustic potash.

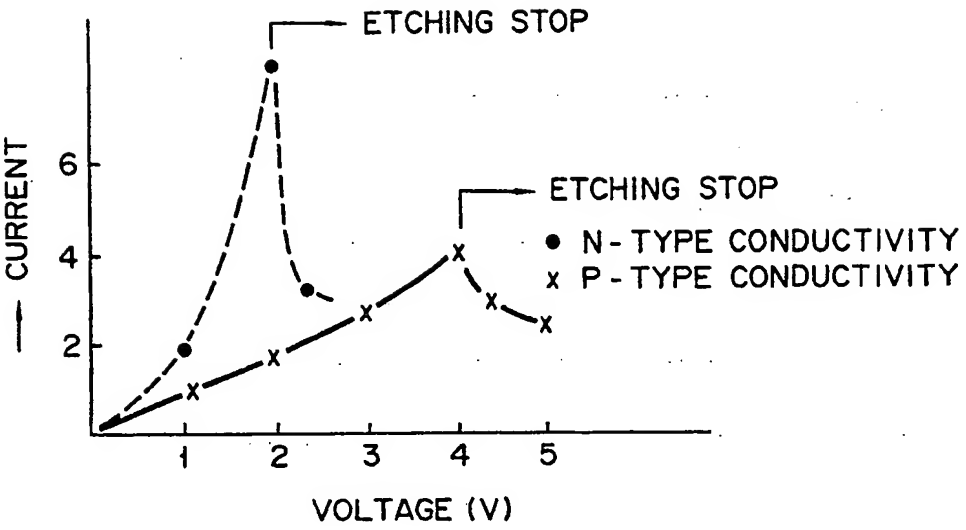
ETCHING STOP
ETCHING STOP
CURRENT
6
4
2
1
2
3
4
5
VOLTAGE (V)
● N-TYPE CONDUCTIVITY
x P-TYPE CONDUCTIVITY

FIG. 1

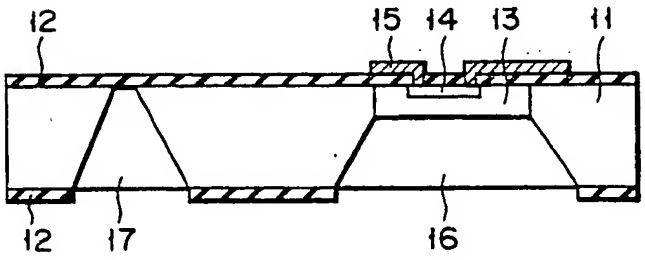
12
15
14
13
11
12
17
16

FIG. 2

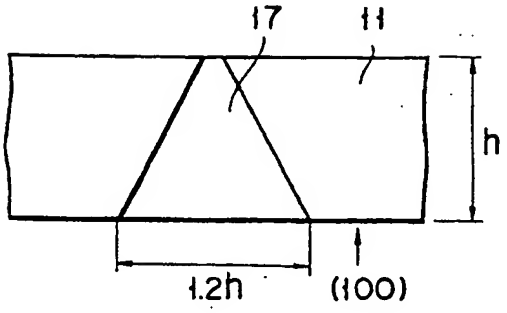

FIG. 3

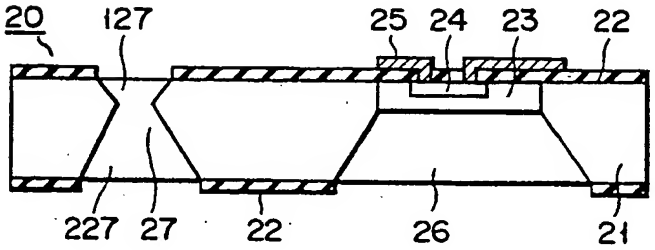

FIG. 4

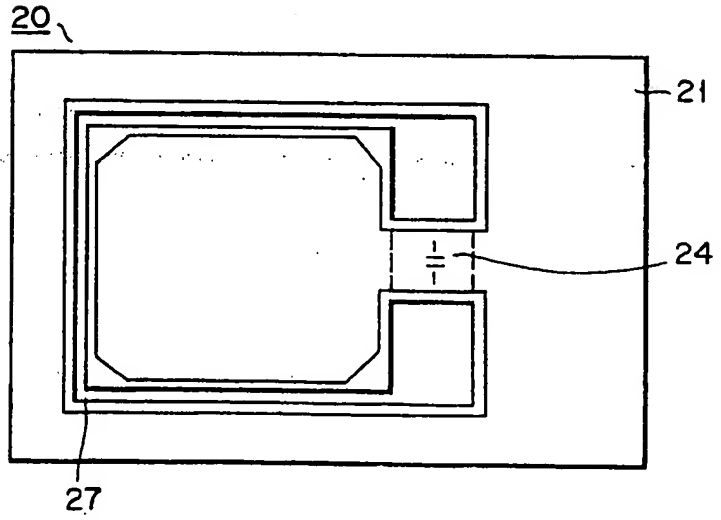

FIG. 5

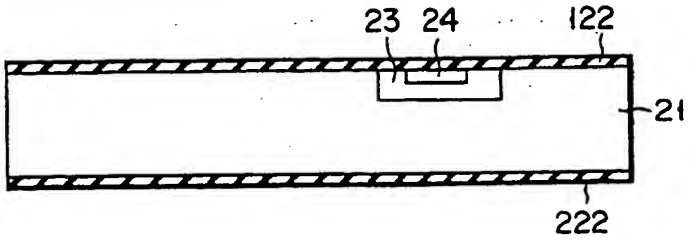

FIG. 6A

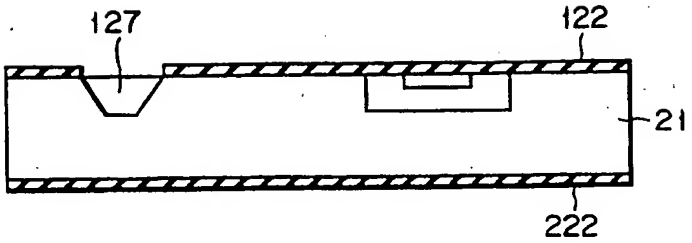

FIG. 6B

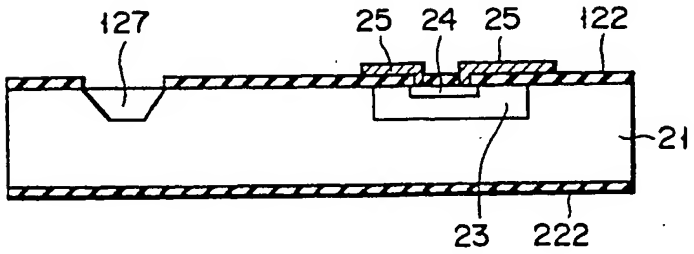

FIG. 6C

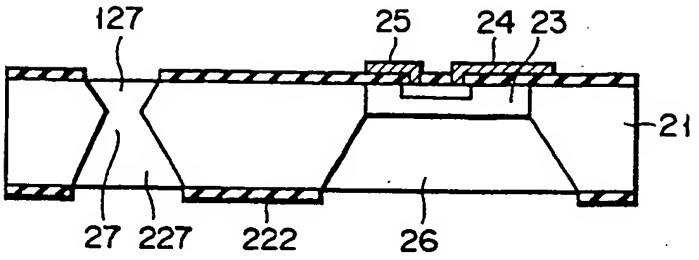

FIG. 6D

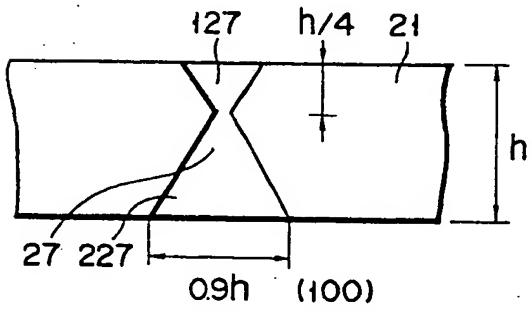

FIG. 7

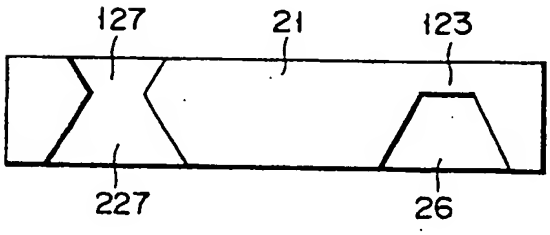

FIG. 8A

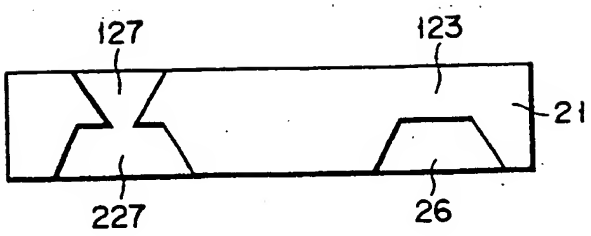

FIG. 8B

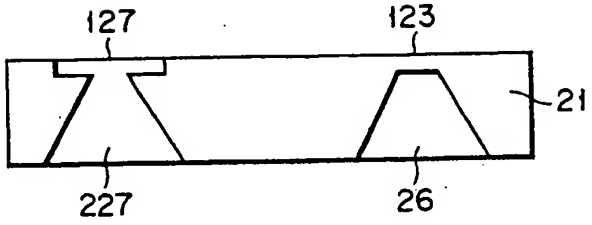

FIG. 8C